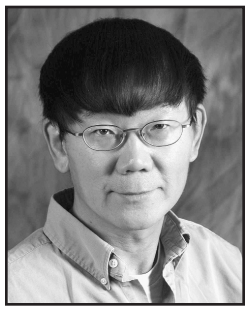
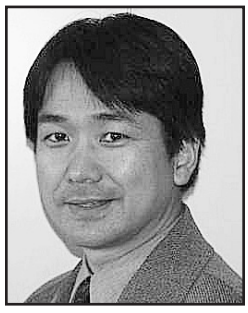
Session 18 Overview

SRAM



Chair: Kevin Zhang, *Intel, Hillsboro, OR*



Associate Chair: Hiroyuki Yamauchi, *Fukuoka Institute of Technology, Fukuoka, Japan*

The ever-growing demand on high-performance multimedia processors continues to drive the performance of embedded SRAM to meet the bandwidth requirement of multiple processing engines in a single die. Meanwhile, low-power consumption in SRAM has also become increasingly important for a wide range of applications in mobile and hand-held devices where extending the battery-life is essential. The low-power requirement can be even more stringent in emerging applications such as environmental and biomedical sensors where the operating voltage has to be scaled down into the subthreshold regime to meet the power constraints. On the technology front, Moore's law continues to drive the scaling of CMOS technology, which brings constant improvement in SRAM density and performance. But the shrinking transistor dimensions also make the memory cell vulnerable to device mismatch due to various sources, including both process variations and fundamental device physics. It is becoming more and more challenging to achieve reliable low-voltage operation and meet both read stability and write margin requirements.

The six papers in this session provide a broad perspective in addressing many challenges facing today's SRAM designers. These papers reveal the latest advancements in some of the key technical areas, including high-frequency scaling for high-end processors, balanced power-performance design for handheld applications, cell-stability enhancement, and SRAM design for ultra-low voltage operation.

Paper 18.1 from IBM, Toshiba and Sony describes the implementation of an L1 cache design for the CELL® Broadband Engine in a 65nm SOI technology. It adopts a large-signal ripple-domino sensing scheme to achieve up to 6GHz operation at 1.3V to meet the processor core requirement. The SRAM design employs a dual-power supply to achieve voltage scalability while maintaining cell stability.

Low leakage power during standby mode is critical to having long-battery life in mobile applications. The conventional SRAM design in this segment needs to significantly tradeoff performance for low-power. Paper 18.2 from Intel reports a 65nm SRAM design for this application. A co-optimization between transistor technology and advanced circuit techniques helps reduce leakage down to 2pA/cell at retention while achieving 1.1GHz performance at nominal voltage.

Techniques for SRAM cell-stability enhancement have been reported before but many of them lose their benefits in manufacturing environments due to process, voltage, and temperature (PVT) variations. Paper 18.3 from Renesas and Matsushita introduces a design to improve the tracking of PVT variations. The benefits are demonstrated using 45nm SRAM cells with a cell size of 0.245μm^2.

The remaining three papers from this session address the emerging applications of ultra-low-voltage operations. Three different SRAM cell topologies ranging from 6T to 10T are explored, reliably operating down to the subthreshold regime. A variety of design techniques in the peripheral circuits assist the ultra-low voltage operation while further reducing the SRAM leakage power. Paper 18.4 from MIT presents bitline leakage gating and built-in redundancy in data sensing. Paper 18.5 from U Minnesota presents data-independent bitline leakage and data-sensing enhancements. Paper 18.6 from U Michigan presents dynamic voltage scaling for read and write margin improvement. The silicon results of these three papers demonstrate the functionality of these designs well below 350mV.

18.1 Implementation of the CELL Broadband Engine™ in a 65nm SOI Technology Featuring Dual-Supply SRAM Arrays Supporting 6GHz at 1.3V **1:30 PM**

J. Pille, IBM, Boeblingen, Germany

The 65nm CELL Broadband Engine™ design features a dual power supply, which enhances SRAM stability and performance using an elevated array-specific power supply, while reducing the logic power consumption. Hardware measurements demonstrate low-voltage operation and reduced scatter of the minimum operating voltage. The chip operates at 6GHz at 1.3V and is fabricated in a 65nm CMOS SOI technology.

18.2 A 1.1GHz 12µA/Mb-Leakage SRAM Design in 65nm Ultra-Low-Power CMOS with Integrated Leakage Reduction for Mobile Applications **2:00 PM**

Y. Wang, Intel, Hillsboro, OR

A low-power high-speed SRAM macro is implemented in an ultra-low-power 8M 65nm CMOS for mobile applications. The 1Mb macro features a 0.667µm^2 low-leakage memory cell and operates with supply voltage from 0.5V to 1.2V. It operates at a frequency of 1.1GHz at 1.2V and 250MHz at 0.7V. Leakage is reduced to 12µA/Mb at the data retention voltage of 0.5V. The measured bitcell leakage from the SRAM array is ~2pA/b at retention voltage with integrated leakage reduction schemes.

18.3 A 45nm Low-Standby-Power Embedded SRAM with Improved Immunity Against Process and Temperature Variations

M. Yabuuchi, Renesas Technology, Itami, Hyogo, Japan **2:30 PM**

A 512kb SRAM module is implemented in a 45nm low-standby-power CMOS with variation-tolerant assist circuits against process and temperature. A passive resistance is introduced to the read assist circuit and a divided V_{DD} line is adopted in the memory array to assist the write. Two SRAM cells with areas of 0.245µm^2 and 0.327µm^2 are fabricated. Measurements show that the SNM exceeds 120mV and the write margin improves by 15% in the worst PVT condition.

18.4 A 65nm 8T Sub-V_t SRAM Employing Sense-Amplifier Redundancy **3:15 PM**

N. Verma, Massachusetts Institute of Technology, Cambridge, MA

A 65nm 256kb 8T SRAM operates in sub-V_t at 350mV. Peripheral assists eliminate sub-V_t bitline leakage without limiting read current, and for a given area, sense-amplifier redundancy reduces read errors from offsets by a factor of five compared with device upsizing.

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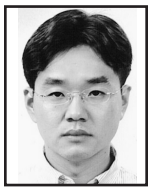

18.5 A High-Density Subthreshold SRAM with Data-Independent Bitline Leakage and Virtual-Ground Replica Scheme **3:45 PM**

T-H. Kim, University of Minnesota, Minneapolis, MN

A 10T SRAM cell with data-independent bitline leakage and a virtual-ground replica scheme allows 1k cells per bitline in subthreshold SRAMs. Reverse short-channel effect is used to improve writability, offer higher speed, reduce junction capacitance, and decrease circuit variability. A 0.13µm, the 480kb SRAM test chip shows a minimum operating voltage of 0.20V.

18.6 A Sub-200mV 6T SRAM in 0.13µm CMOS **4:15 PM**

B. Zhai, University of Michigan, Ann Arbor, MI

A deep-subthreshold 6T SRAM functions from 1.2V to 193mV and is fabricated in an industrial 0.13µm CMOS technology. It provides greater than 2× energy-efficiency improvement over the previously proposed MUX-based subthreshold SRAM designs while using half the area. Adjustable footer and headers are introduced, as well as body-bias techniques to allow low-voltage operation.